Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEVEN E. RICE

Appeal No. 1998-0368
Application No. 08/632,183

ON BRIEF

Before BARRETT, RUGGIERO and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection[1] of claims of 1 to 3, which constitute all the claims in the application.

The disclosed invention is related to an inter-processor data transfer management system for increasing overall throughput for both processors. The invention provides an interface circuit between the requesting processor bus and the

[1] An amendment after the final rejection was filed as paper no. 15 and was approved for entry by the Examiner [paper no. 16].

responding processor bus which, in response to a data transfer request from the requesting processor, acknowledges the request so that the requesting processor may continue to run without stalling. The interface circuit then arbitrates for the bus of the responding processor and completes the data transfer between the interface circuit and the responding processor. The interface circuit then advises the requesting processor that it is ready for another request, and upon receipt of another request the interface circuit completes the prior request with the requesting processor. The interface circuit comprises storing means for the data to be written or read and for the address of the location. The interface circuit also has a control means for managing the requests from the processors. The invention is further illustrated by the following claim.

1. An interface circuit for inter-processor data transfer management comprising:

means coupled between a requesting processor bus and a responding processor bus for storing in response to a transfer request initiated by the requesting processor an address and data, the address being an access address to the responding processor and the data being data from the requesting processor for storage at the access address for a write request or data from the responding processor for transfer from the access address for a read request; and

means coupled between the requesting processor bus and the responding processor bus for controlling the storing means and for communicating with requesting and responding processors so that the processors are decoupled from the data transfer in that the transfer request by the requesting processor for access to the responding processor is acknowledged by the controlling means so that the requesting processor may continue its processing until an interrupt is received from the controlling means indicating that the controlling means has completed the request and is ready to receive another request, and the controlling means arbitrates for access to the responding processor bus to complete the data transfer between the responding processor and the storing means so that the responding processor may continue its processing while the data transfer takes place;

whereby the interface circuit controls the data transfer between the requesting and responding processors so that the processors do not stall during such data transfer.

The references relied on by the Examiner are:

Mercer et al. (Mercer)	4,926,375	May 15, 1990
Mizukami	5,309,567 (Filing date: Jan. 24, 1992)	May 3, 1994
Foster et al. (Foster '570)	5,327,570 (Filing date: Jul. 22, 1991)	Jul. 5, 1994
Foster et al. (Foster '654)	5,410,654 (Filing date: Jul. 22, 1991)	Apr. 25, 1995

Claims 1 stands rejected under 35 U.S.C. § 103 over Foster '570, Foster '654 and Mizukami, while for claims 2 and 3, the Examiner adds Mercer to the combination.

Reference is made to Appellant’s brief and the Examiner's answer for their respective positions.

OPINION

We have considered the record before us, and we will reverse the rejection of claims 1 to 3.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467
(1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. System., Inc. v.

Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

Furthermore, the Federal Circuit states that "[the] mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fitch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. V. SGS Importers Int'l, 73 F.3d 1087, 37 USPQ 2d at 1239 (Fed. Cir. 1995), citing W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d
at 1551, 1553, 220 USPQ at 311, 312-13 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Analysis

We take claim 1 first. Reviewing the record, we find that the Examiner, in his rejection of the claim over Foster '570, Foster '654 and Mizukami [answer, pages 3 to 4] and his response to Appellant's arguments [answer, pages 7 to 10], has missed the claimed limitation of "means . . . for . . . storing . . . an address . . ., the address being an access address to the responding processor" (emphasis added). We agree with Appellant that, in Foster '570 (even with Foster '654), "[t]here is no direct processor to processor data transfer" [brief, page 4] (emphasis added). We note that Foster '570 and Foster '654 both relate to the same system and have a different architecture from Appellant's architecture. The data do not flow directly among the various processors (i.e., among the card processors and/or I/O processors or across the card processors and I/O processors); instead, the data flow through the local memories and the global memories via the local and the global buses. Indeed, the main object of the two Foster patents is to provide efficient bandwidth utilization of the shared system (global bus 24 and global memory 26) in this indirect data transfer among the processors. See also Foster '570 at col. 5, lines 25 to 41.

We note that the Examiner is correct in that Mizukami provides a means for direct data transfer between the two processors, see figs. 1 and 2. However, the data controlling function in Mizukami is performed by the processors themselves,
and not by the interface circuit (as claimed), see col. 2, lines 3 to 12.

Therefore, we do not sustain the obviousness rejection of claim 1 over Foster ‘570, Foster ‘654 and Mizukami.

With respect to claims 2 and 3, the Examiner adds Mercer to the combination of Foster ‘570, Foster ‘654 and Mizukami. We note that claims 2 and 3 each has a limitation similar to that discussed above, see “setting an access address in the responding processor” (claim 2) and “setting an access address to a first location on the responding processor (claim 3).” We find that the additional reference to Mercer does not cure the deficiency noted above. Therefore, we also do not sustain the obviousness rejection of claims 2 and 3 over Foster ‘570, Foster ‘654, Mizukami and Mercer.

In conclusion, the Examiner's decision rejecting claims 1 to 3 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE E. BARRETT Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

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